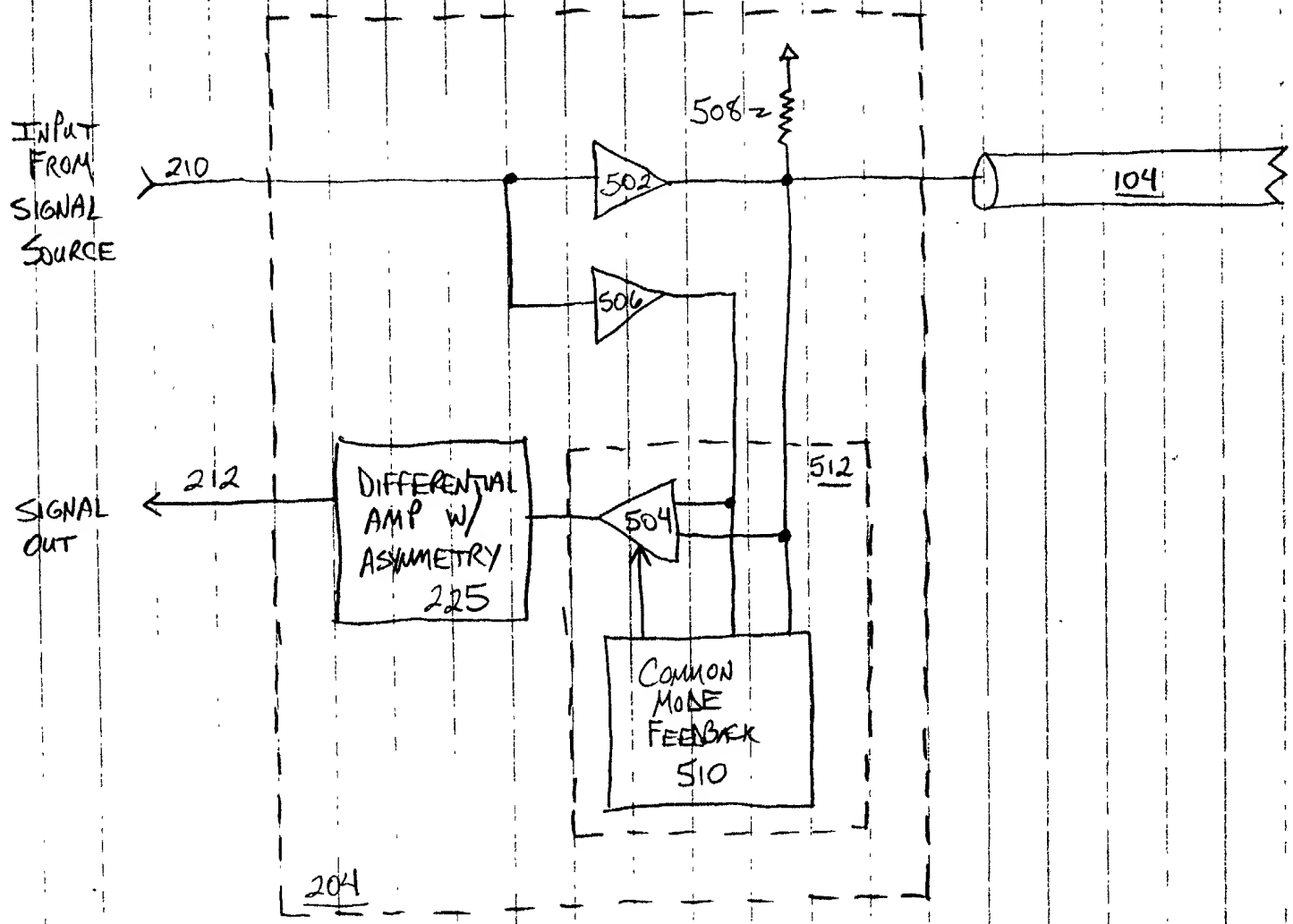
INPUT FROM SIGNAL SOURCE
210
502
508
104
506
212
SIGNAL OUT
DIFFERENTIAL AMP W/ ASYMMETRY 225
504
512
COMMON MODE FEEDBACK 510
204

FIGURE 1

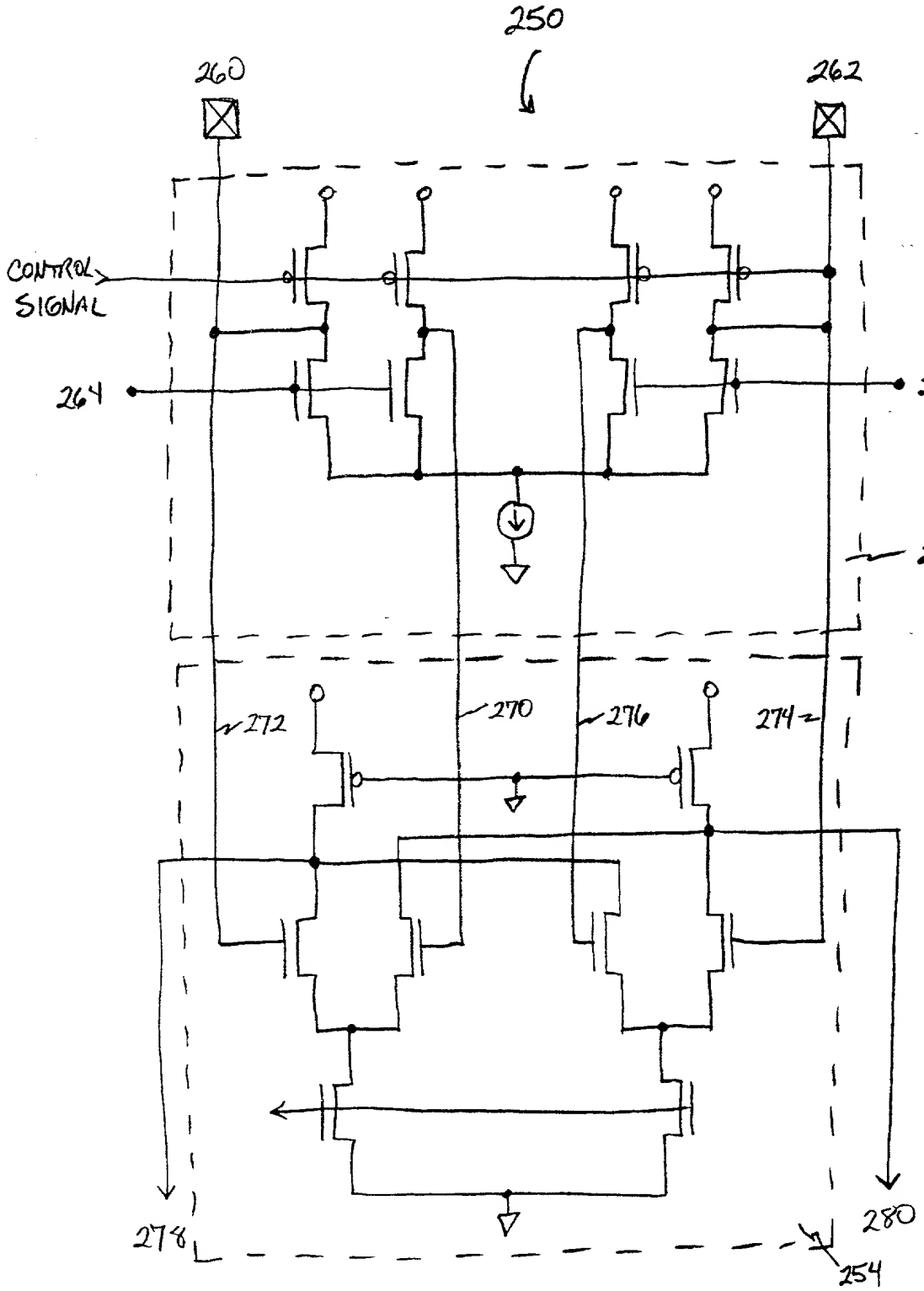

FIGURE 2
(PRIOR ART)

Docket: 03656.0050

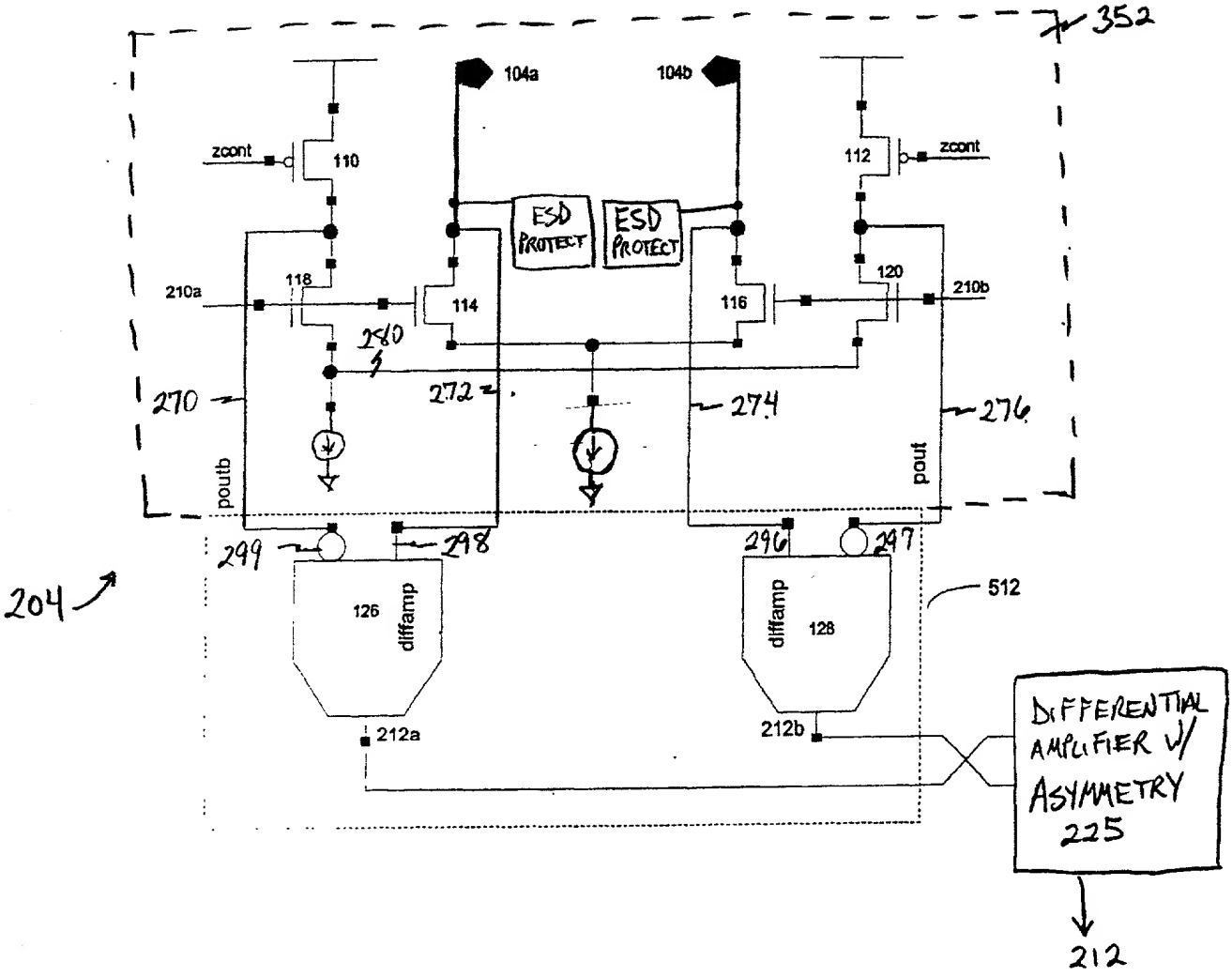

FIGURE 3

Docket No. 03560.0050

126

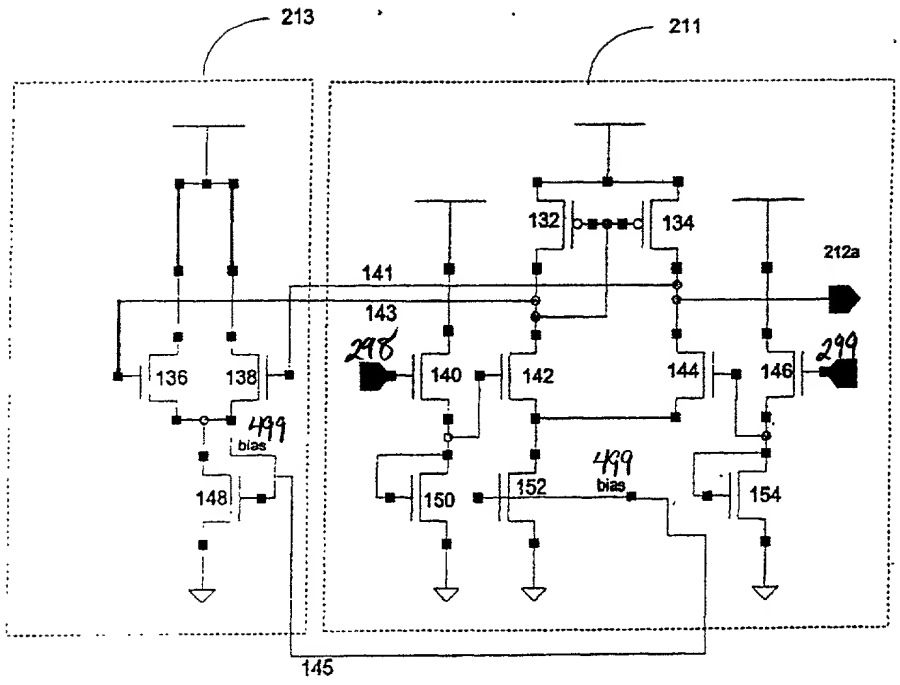

FIGURE 4

09656930 - 112004

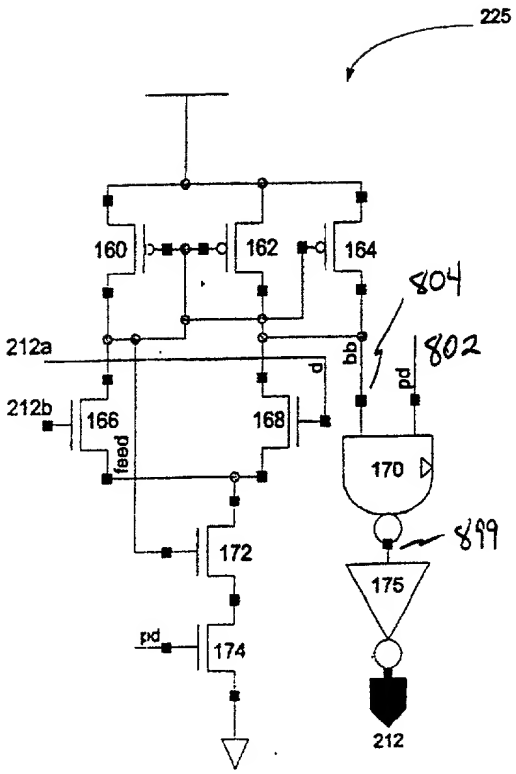

FIGURE 5

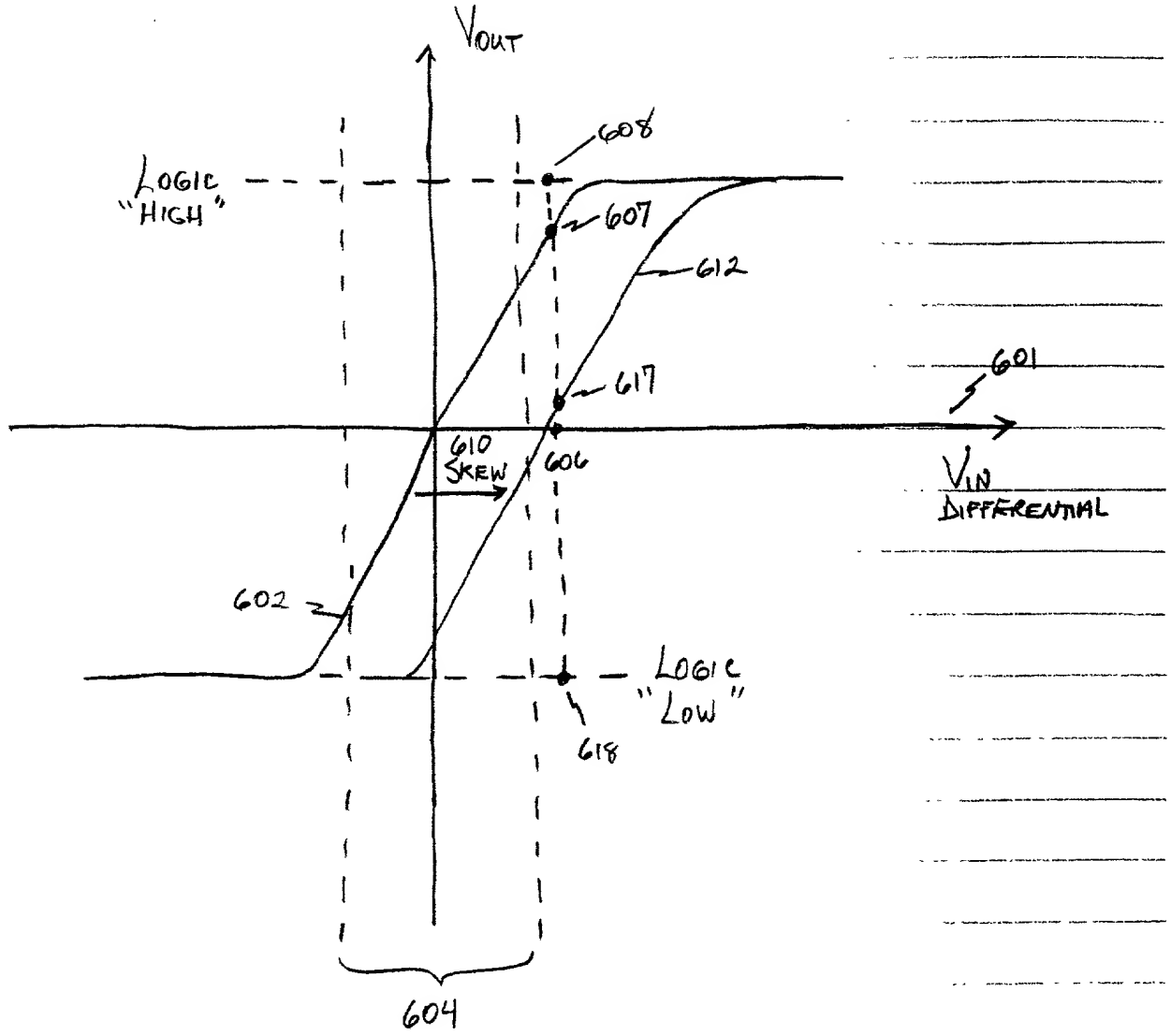
V_{OUT}
LOGIC "HIGH"
608
607
612
617
601
610 SKEW
606
V_{IN} DIFFERENTIAL
602
LOGIC "LOW"
618
604

FIGURE 6

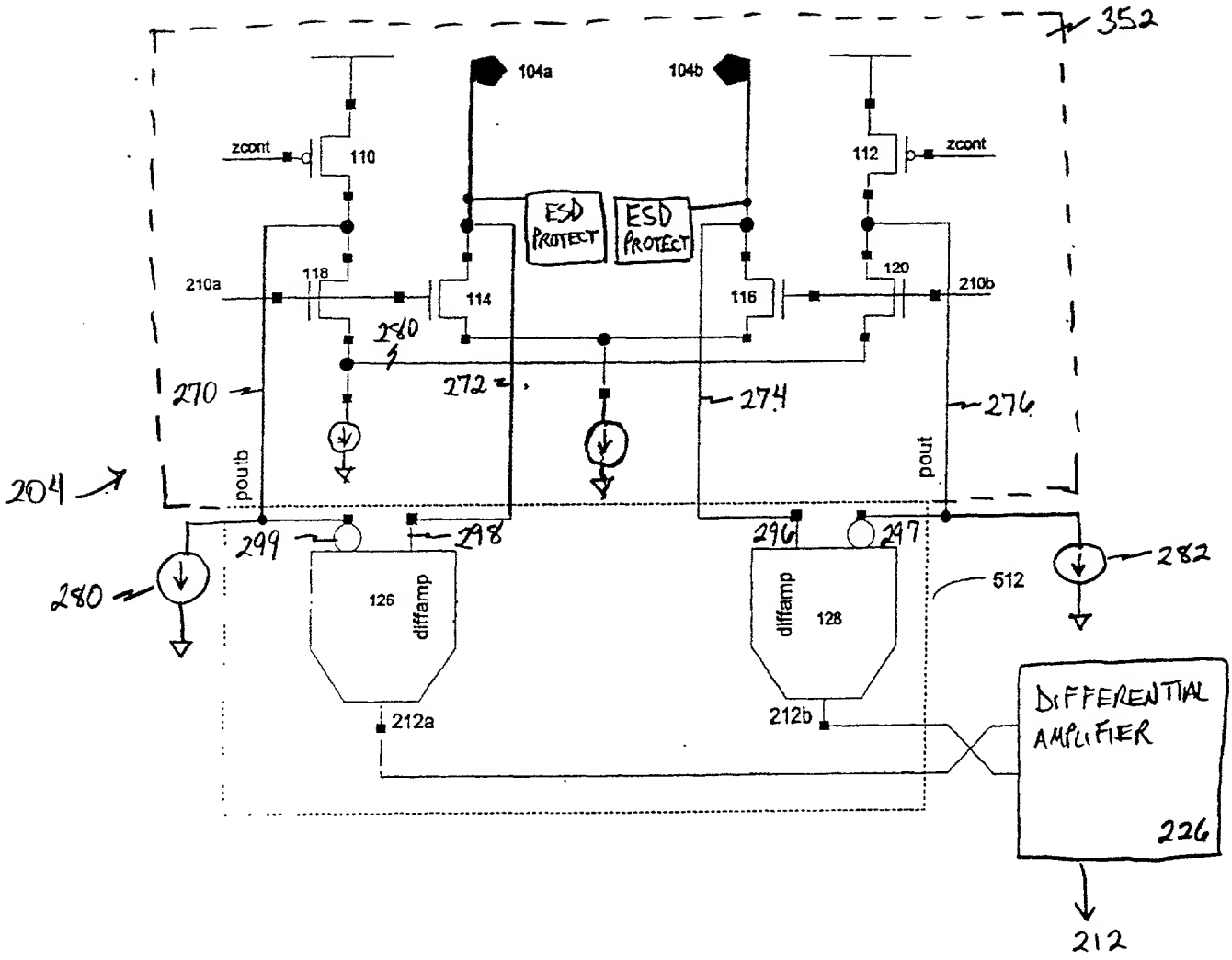
352
104a
104b
zcont
110
112
zcont
ESD PROTECT
ESD PROTECT
210a
118
114
116
120
210b
280
270
272
274
276
204
poutb
pout
299
298
296
297
282
280
512
126
diffamp
diffamp
128
212a
212b
DIFFERENTIAL AMPLIFIER
226
212

FIGURE 7

US 6,252,465 B1 Jun. 26, 2001

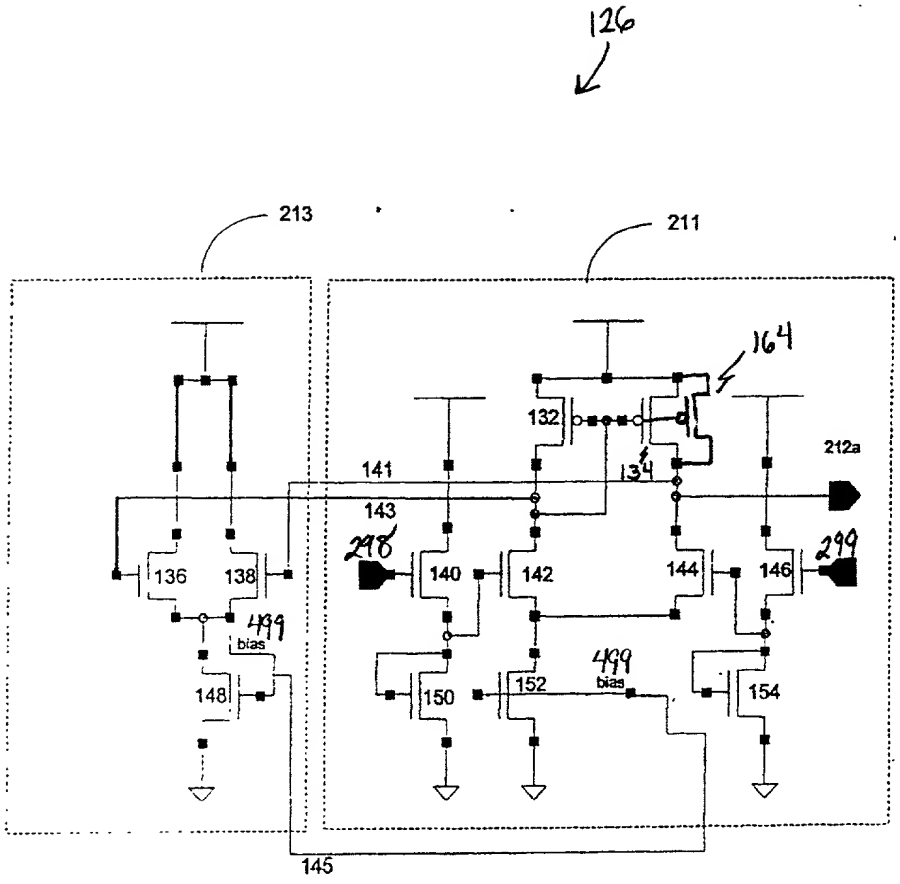

FIGURE 8

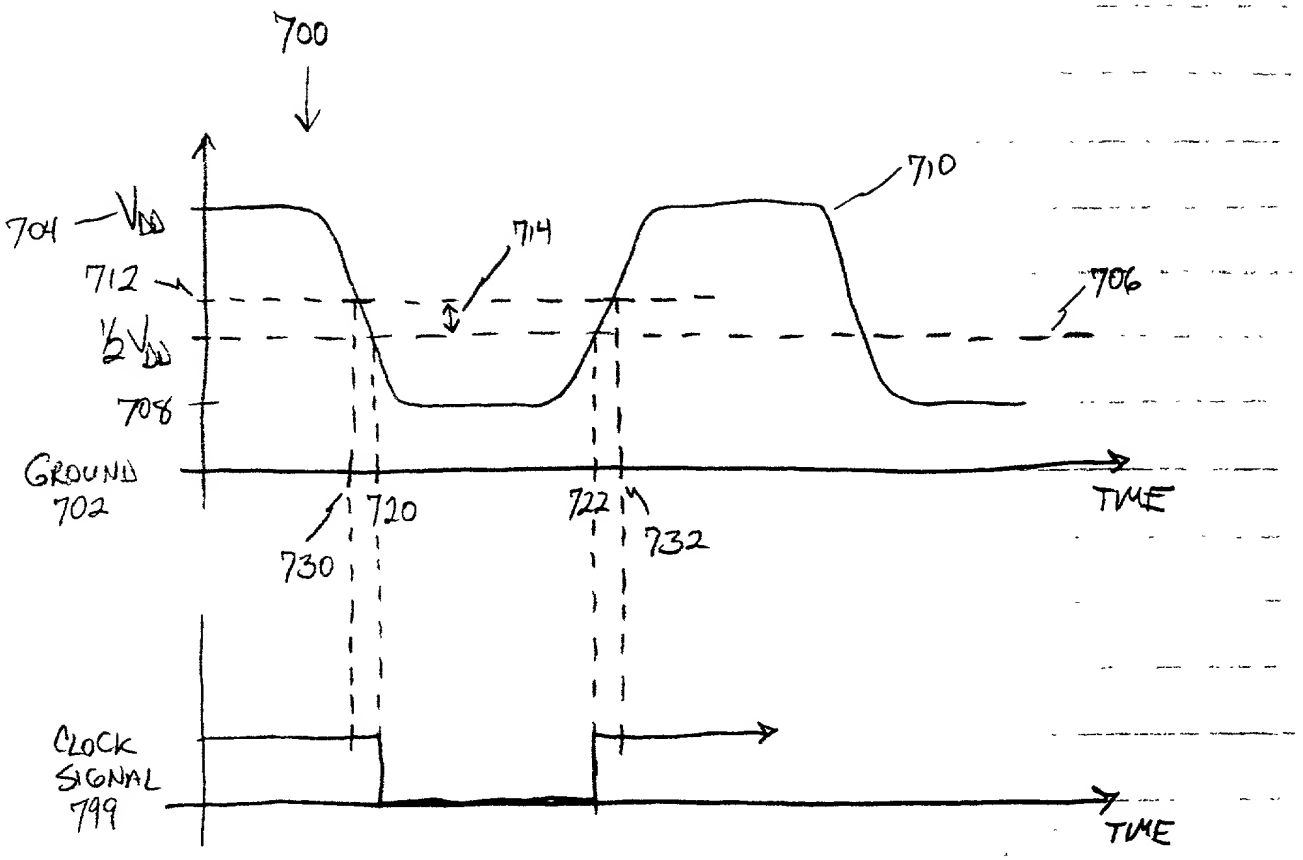

FIGURE 9

Attorney Docket No. 10559-1200

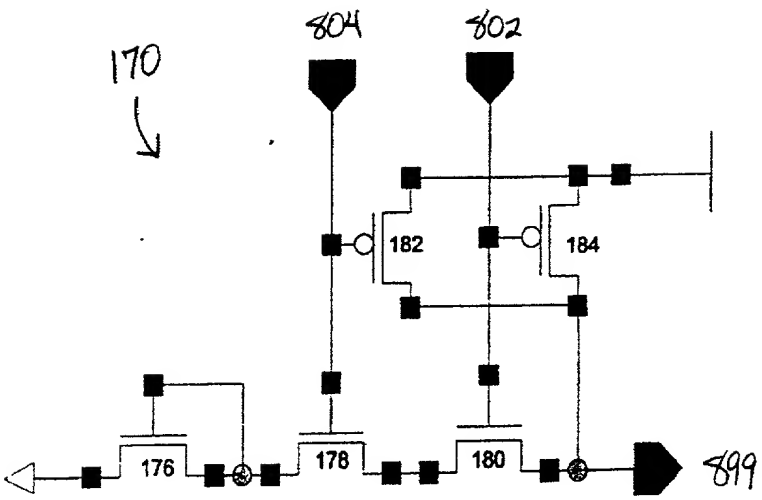

FIGURE 10A

Toggle "Bass Boost"

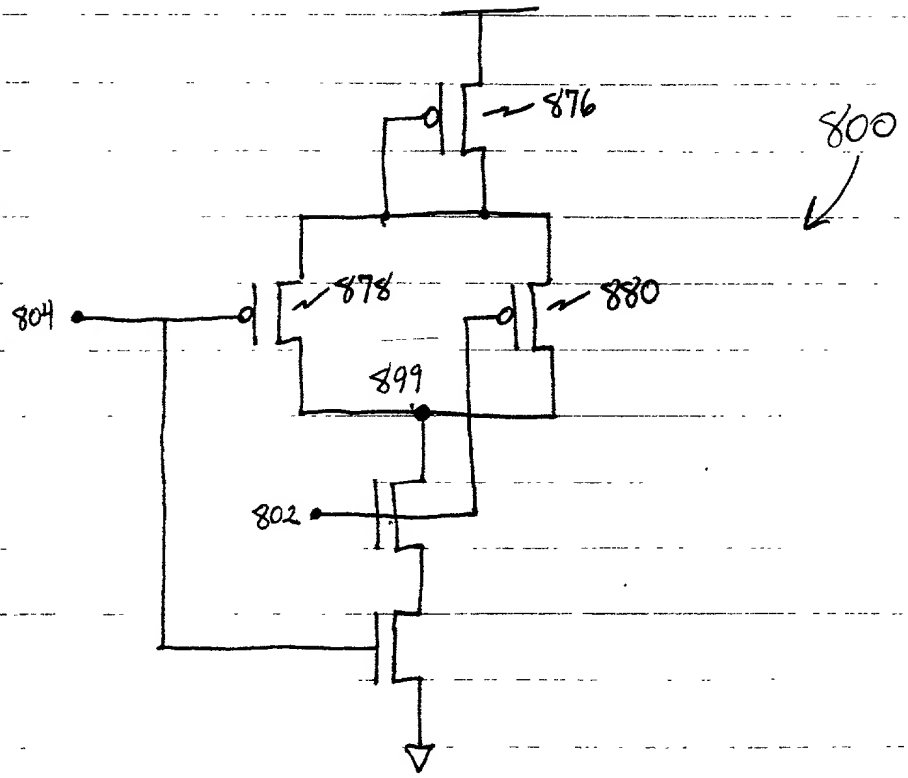

FIGURE 10B

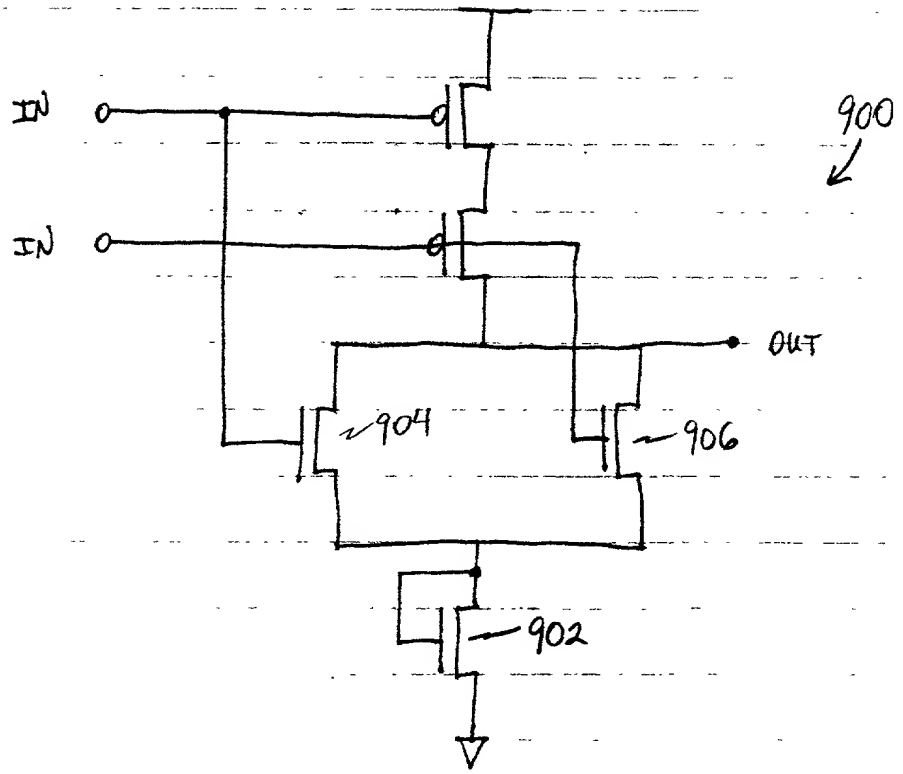

FIGURE 11A

Document1 - 09/23/04

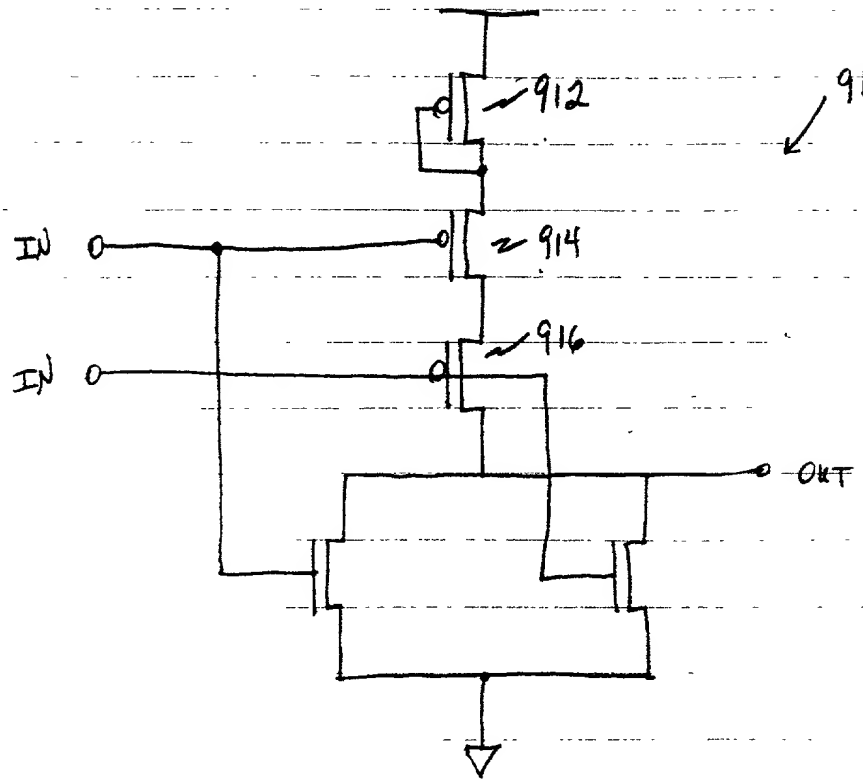

FIGURE 11B

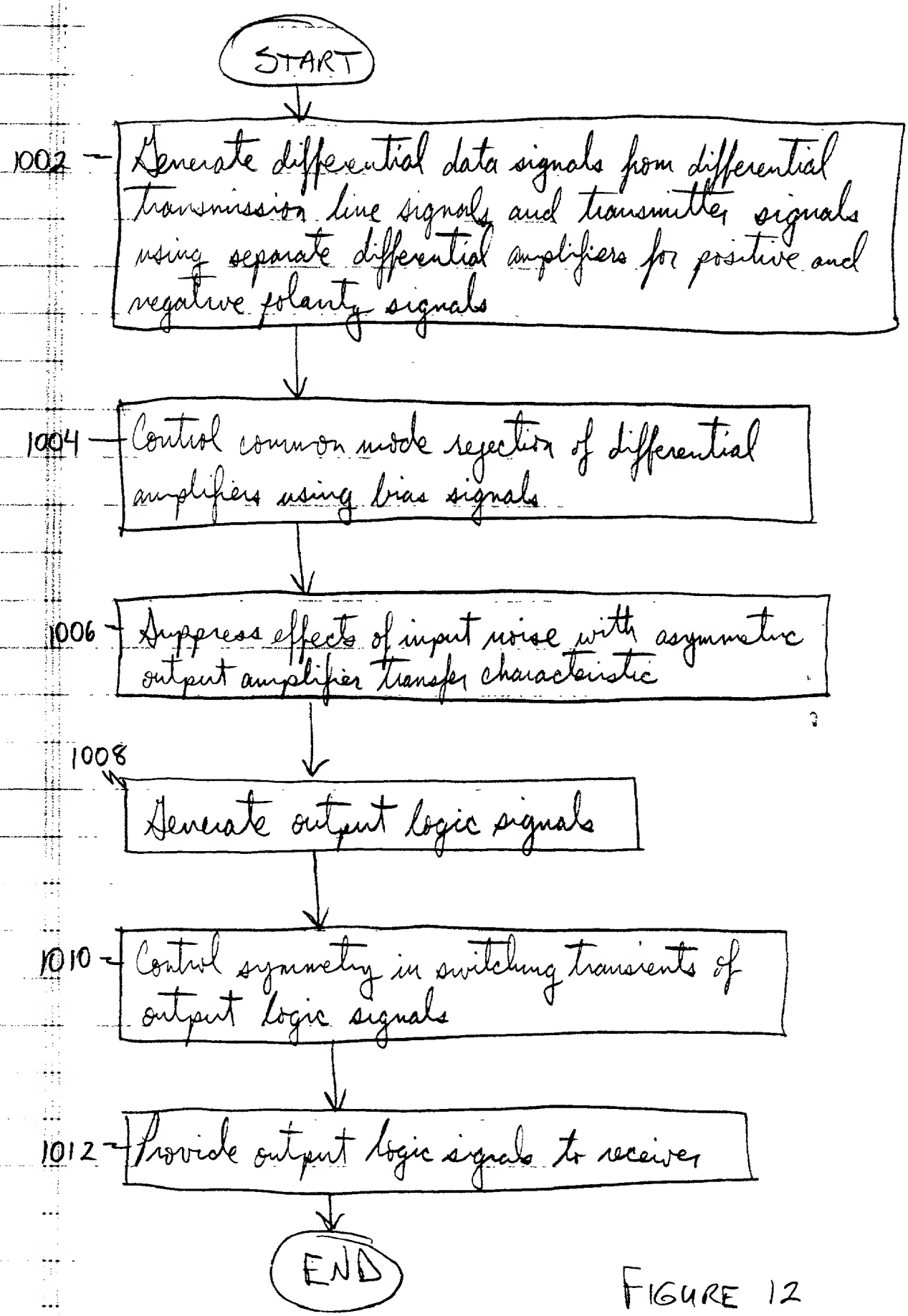
START
1002
Generate differential data signals from differential transmission line signals and transmitter signals using separate differential amplifiers for positive and negative polarity signals
1004
Control common mode rejection of differential amplifiers using bias signals
1006
Suppress effects of input noise with asymmetric output amplifier transfer characteristic
1008
Generate output logic signals
1010
Control symmetry in switching transients of output logic signals
1012
Provide output logic signals to receiver
END

FIGURE 12